Director
Siliguri Institute of Technology

SILIGURI INSTITUTE OF TECHNOLOGY

ELECTRONICS & COMMUNICATION ENGINEERING

COURSE FILE

1ST SEM, 4TH YEAR, 2016 (GR. A)

PAPER NAME : *Microelectronics and VLSI Designs* (EC-702) & VLSI Design Lab (EC- 792)

PAPER CODE : EC 702 & EC 792

Course File

Course Title: ***Microelectronics and VLSI Designs*** **(EC- 702) &VLSI Design Lab (EC- 792)**

Semester: **1st Year 4th, 2016**

Name of the Faculty: **Prof. Manas Kumar Parai & Prof. Saroj Mondal**

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Class Schedule:

Lecture				Practical	
Tuesday	**Wednesday**	**Thursday**	**Friday**	**Wednesday**	**Thursday**
11.40am – 12.30pm	10.00am – 10.50am	2.10pm – 3 pm	2.10pm – 3 pm	10.50am – 1.20pm	10.50am – 1.20pm

- An additional Lecture per week (which is not as per university syllabus) has been incorporated for facilitating better understanding and coverage of the syllabus.

Hours for meeting students:

Tuesday	**Thursday**	**Saturday**	**Other Days**
1.30pm – 2.45pm	3pm – 4pm	1.30pm – 4pm	1.30pm – 2pm or by appointment

i) Course Objective

Student will possess sufficient knowledge about the principles of VLSI design, Fabrication Process and simulate large-scale Digital and Analog Integrated Circuits.

ii) Course Outcomes

i. After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes.

The student will be able to:

	Outcomes	**Target**
EC702.1	**Describe**the basic concept of VLSI design: Microelectronic evaluation, Scale of Integration, Types of VLSI Chips, different design domains and design principles. [B.T. LEVEL 1]	70% marks

EC702.2	**Understand** Silicon Semiconductor Technology and CMOS processing technology: P-well, N-well, Twin Tub process, layout Design rules. [B.T. LEVEL 2]	70% marks
EC702.3	**Implement** CMOS logic circuits, Complex logic circuits, Advanced Logic circuits and different sequential CMOS logic circuits. [B.T. LEVEL 3]	60% marks
EC702.4	**Test** different combinational and sequential logic circuits and verify their behavior with Spice Simulation and EDA tools for VLSI Design. [B.T. LEVEL 5]	75% marks
EC702.5	**Design** and develop CPLD/FPGA based small prototype. [B. T. LEVEL 6]	95% marks

ii. Once the student has successfully complete this course, he/she must be able to answer the following questions or perform/demonstrate the following:

Sl.	Question	BT Level
1.	**Describe** the flow chart of VLSI Design Flow.	1
2.	**Explain** with neat diagram the basic steps involved in fabrication Process flow.	2
3.	**Explain** the Stick Diagram of 3-input NAND Gate.	2
4.	**Utilize** the operation of CMOS Inverter circuit and Show the Voltage Transfer Characteristic.	3
5.	**Apply** CMOS technology to implement Half Adder, Full Adder, D FF.	3
6.	**Construct** a Resistor using Switched Capacitor.	3
7.	**Verify** DC, AC and Transient response of different logic gates using Spice Simulation and EDA tools.	5
8.	**Test** the operations of CMOS full adder, Flip-Flops, Counter, and Registers.	5
9.	**Design**12-bit CPU using VHDL to check its functions and validate on FPGA/CPLD.	6

iii) Module Layout

Module	Lecture Hours	Laboratory hours
I. Introduction to VLSI Design	8 HRS.	6HRS.
II. Microelectronic Processes for VLSI Fabrication	10 HRS.	-
III. CMOS for Digital VLSI Circuits	12 HRS.	24HRS
IV. Analog VLSI Circuits	10 HRS.	-

iv) Textbooks

1. Digital Integrated Circuit, J. M. Rabaey, Chandrasan, Nicolic, Pearson Education.
2. CMOS Digital Integrated Circuit, S. M. Kang & Y. Leblebici, TMH.
3. Modern VLSI Design, Wayne Wolf, Pearson Education.
4. Advance Digital Design Using Verilog, Michel D. Celliti, PHI
5. M.J.S Smith, Application Specific Integrated circuits, Pearson.
6. P.J Anderson, The designer’ s guide to VHDL, Morgan Kaufman, 2nd edition, 2002.
7. W. Wolf, Modern VLSI Design: Systems on silicon, Pearson
8. G. Hatchel and F. Somenzi, logic Synthesis and verification Algorithms,Kluwer,1998

Reference books:

1. Digital Integrated Circuits, Demassa & Ciccone, John Willey &Sons.
2. Modern VLSI Design: system on silicon, Wayne Wolf; Addison Wesley Longman Publisher
3. Basic VLSI Design, Douglas A. Pucknell & Kamran Eshranghian, PHI
4. CMOS Circuit Design, Layout & Simulation, R. J. Baker, H. W. Lee, D.E. Boyee, PHI
5. CMOS Analog Circuit Design by P.E. Allen & D.R. Holberg; OUP
6. J. Bhasker, A VHDL Primer, BS Publications/Pearson Education.

(v) Evaluation Scheme

1) Theory

Evaluation Criteria	Marks
Internal Exam*	15
Quiz Test	10
Attendance	5
University Exam	70
Total	100

* Two internal examinations are conducted; based on those two tests, average of them are considered in a scale of 15.

University Grading System:

Grade	Marks
O	90% and above
E	80 – 89.9%
A	70 – 79.9%
B	60 – 69.9%
C	50 – 59.9%
D	40 – 49.9%
F	Below 40%

2) Laboratory

Evaluation Criteria	Marks
Internal Exam*	40
University Exam	60
Total	100

*****Internal Evaluation will be based on daily lab performance as per the following schedule:

Expt. No.	Experiment Name	Schedule	Marks (40)
1	Familiarity with Spice simulation tool& EDA tools	6HRS.	6
2	Spice Simulation of Inverter , NAND , NOR Gates	6 HRS.	6
3	Design of CMOS XOR/XNOR Gates	3 HRS.	6
4	Design of CMOS Full adder	3 HRS.	5
5	Design of CMOS Flip flops (R-S ,D , J-K)	3 HRS.	5
6	Design of 8 bit synchronous Counter	3 HRS.	5
7	Design of 8 bit bi-directional register	3 HRS.	5
8	Design of a 12 bit CPU with few instructions and implementation and validation on FPGA	3 HRS.	2

Course target attainment levels:

Attainment Level	Inference	Marks
Attainment Level 1	50% of the students have attained more than the target level of that CO	1
Attainment Level 2	60% of the students have attained more than the target level of that CO	2
Attainment Level 3	70% of the students have attained more than the target level of that CO	3

Overall Course Attainment Target (70% of university and 30% of the internal exam) will be =Attainment Level 3

Target has been set on the basis of last year's performance / result by the students, student quality this year and difficulty level of the course.

(vi) Mapping of Course Outcomes and Program Outcomes:

Course Outcomes	Program Outcomes (POs)												PSOs	
	1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12	1.	2.
EC 702.1	1	2	0	2	0	0	0	0	0	0	0	0	1	0
EC 702.2	1	2	0	2	0	0	0	0	2	0	0	0	1	2
EC 702.3	2	2	0	3	0	0	0	0	2	0	0	0	2	2
EC 702.4	1	2	0	3	0	0	0	0	2	0	0	0	2	2
EC 702.5	1	0	0	3	0	0	0	0	2	0	0	0	1	2
EC 702	1	2	0	3	0	0	0	0	2	0	0	0	1	2

- CO1, 2, 4 & 5 minimally satisfy whereasCO3 partially satisfies the application of knowledge of mathematics, science, engineering fundamentals to the solution of complex engineering problems (PO1).
- CO1, 2, 3 & 4 partially satisfies the ability of the student to identify, formulate, and analyze engineering problems to arrive at substantiated conclusions (PO2).
- CO3, 4 & 5 fully satisfies &1, 2 partially satisfy the research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions in the field of Electronics & Communication Engineering. (PO4).
- CO2, 3, 4 & 5 partially satisfies the student's ability to function effectively as an individual and as a member in a team (PO9).

(vii) Delivery Methodology

Outcome	Method	Supporting Tools	Demonstration
EC 702.1	Structured (Partially Supervised Whole-Class Grouping)	Video Lecture, NPTEL materials	Basic concept of VLSI design
EC 702.2	Structured (Partially Supervised Whole-Class Grouping)	Video Lecture, NPTEL materials	Microelectronic Processes for VLSI Fabrication
EC 702.3	Structured (Partially Supervised Whole-Class Grouping)	Video Lecture, NPTEL materials	CMOS Analog and digital logic circuits
EC 702.4	Structured (Partially Supervised Independent work)	Whiteboard & Marker, PPT &Software Based	Simulation using T-Spice & Xilinx
EC 702.5	Structured (Partially Supervised Independent work)	Whiteboard & Marker, PPT &Software Based	Simulation using T-Spice & Xilinx

(viii) Assessment Methodology

Outcome	Assessment Tool	Specific Question/activity aligned to the Outcome
EC 702.1	Internal Test	Q1. Draw the flow chart of VLSI Design Flow and Explain.
	Quiz	1. What is meant by the term VLSI? A device containing between (a) 10^3 and 10^5 transistors (c) 10^7 and 10^9 transistors (b) 10^5 and 10^7 transistors(d) 10^9 and 10^{11} transistors 2. Sub threshold operation occurs in (a) Strong inversion region (c) Saturation region (b) Weak inversion region (d) Cut-off region
	University Exam	1. Explain the basic block diagram of FPGA with diagram.

EC 702.2	Internal Test	1. Explain with neat diagram the basic steps involved in fabrication Process flow
	Quiz	1. Material used for the fabrication of gate in modern MOSFET is (a) Highly pure si (c) Epitaxial Si (b) Highly pure SiO_2 (d) Highly doped polysilicon 2. Photo-etching is a process of (a) Selective removal of layer (c) Removal of photo-resist (b) Diffusion of impurities (d) Making dicing marks
	University Exam	1. Show the different steps to fabricate a CMOS Inverter
EC 702.3	Internal Test	1. Explain the operation of CMOS Inverter circuit and Show the Voltage Transfer Characteristic.
	Quiz	i. AND terms are realized by which connections of NMOS in PDN (a) Series (c) parallel (b) Cascade (d) Either Series or Parallel ii. Which one effect does not cause any deviation of a Current Mirror circuit from the ideal situation? (a) Channel length modulation (c) imperfect geometrical matching (b) Threshold offset between the two transistors (d) DIBL effects
	University Exam	1. Realize a 2:1MUX using CMOS Transmission gate. 2. Design two inputs X-OR gate using CMOS Transmission gate. 3. Realize a function using CMOS Transmission gate.
EC 702.4	Quiz	i. The full form of VHDL is (a) Very High Digital Logic (b) Verilog Hardware Description Language (c) Very High Speed Digital Logic (d) None of these ii. In VHDL, Sequential statements are defined in the (a) Architecture (b) Process (c) Package (d) None of these
	Lab	1. Using T-spice obtain the transient analysis of the CMOS Inverter. 2. Write the VHDL code for a Half Adder Circuit in Dataflow style of modeling.
EC 702.5	Quiz	i. In VHDL, Components must be declared (a) Within the architecture body (b) Anywhere in the program (c) In a separate VHDL file (d) Within the entity declaration

		ii. The if-else statements must be (a) Within a process block (b) Within the architecture body (c) Under the entity declaration (d) Within a while loop
	Lab	Design of a 12 bit CPU with few instructions and implementation and validation on FPGA

(ix) A. Weekly Lesson Plan

Week	Lectures	Practical	Quiz
1	VLSI Design Concepts, Moor's Law, Scale of Integration (SSI, MSI, LSI, VLSI, ULSI, Types of VLSI Chips (Analog & Digital VLSI chips)	Familiarity with Spice simulation tool& EDA tools	-
2	ASIC, PLA, FPGA, Design principles (Digital VLSI –Concept of Regularity, Granularity etc), Design Domains (Behavioral, Structural etc.)	Familiarity with Spice simulation tool& EDA tools	-
3	Silicon Semiconductor Technology-An Overview, Wafer processing, Oxidation, Epitaxial deposition, Ion-implantation & Diffusion, Cleaning, Etching, Photo-lithography – Positive & Negative photo-resist, Basic CMOS Technology – (Steps in fabricating CMOS)	Spice Simulation of Inverter	**Quiz1:** Based on CO1. **Topic:** Scale of Integration, VLSI Design flow, Programmable Logic
4	Basic n-well CMOS process, p-well CMOS process, Twin tub Process	Spice Simulation of Inverter	-

5	Layout Design Rule: Stick diagram with examples, CMOS inverter characteristics.	Design of CMOS XOR/XNOR Gates	**Quiz2:** Based on CO2. **Topic:** Fabrication Process, Design Rule.
6	NAND & NOR Gates, CMOS logic circuits, Complex logic circuits	Design of CMOS Full adder	-
7	CMOS Full Adder, CMOS Transmission GATE, Sequential CMOS logic circuits, SR Latch circuit.	Design of CMOS Flip flops (R-S ,D , J-K)	-
8	Clocked JK Latch/ Master-Slave JK, CMOS D-latch & Edge triggered flip-flop, Analog VLSI design steps, Basic building blocks of Analog VLSI chips, MOS switch, Active load / resistors; Voltage dividers.	Design of 8 bit synchronous Counter	**Quiz3:** Based on CO3. **Topic:** Design of Digital and Analog VLSI circuits (Theoretical).
9	CMOS Current source & sink, CMOS Differential amplifier; Output amplifiers [Basic circuits only].	Design of 8 bit bi-directional register	**Quiz4:** Based on CO4. **Topic:** Design of Digital and Analog VLSI circuits (Lab Oriented).
10	CMOS OPAMP, Switched capacitor filter.	Design of a 12 bit CPU with few instructions and implementation and validation on FPGA	
11	Discussion of WBUT question papers, Revision & Doubt Clearing		**Quiz5:** Based on CO5. **Topic:** Design of Prototype.

B. Daily Lesson Plan

MODULE: 1 Title: **Introduction to VLSI Design** Day 1, Tuesday, Date: 02.08.16 [11.40am to 12.30pm]
CONTENTS Introduction to VLSI Design Concepts. Discussion on course objectives and outcome, text & reference books, evaluation scheme and weekly lesson plan.
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To gather the knowledge of Different VLSI designs Flow.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Draw the flow chart of VLSI Design Flow and Explain [L1] 2. What are different VLSI design styles? Explain each of them. [L2]
Remarks, if any

MODULE: 1 Title: **Introduction to VLSI Design** Day 2, Wednesday, Date: 03.08.16 [10.00am to 10.50am]
CONTENTS Moor's Law, Scale of Integration (SSI, MSI, LSI, VLSI, ULSI)
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To recognize the application areas of Moore's Law and the course in diverse disciplines. 2. To understand the level of complexity due to integration of analog and digital circuits embedded in single integrated circuit.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What is Moore's Law? Justify it. [L1]. 2. Does the Moore's law satisfy the modern integration Technology? [L2]
Remarks, if any

MODULE: 1 Title: **Introduction to VLSI Design** Day 3, Thursday, Date: 04.08.16 [2.10pm to 3.00pm]
CONTENTS Types of VLSI Chips (Analog & Digital VLSI chips, General purpose, ASIC)
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To understand basic difference between analog and digital VLSI chip.

2. To understand different types of ASICs available.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What is ASIC? [L1] 2. What are the different architectures available for the ASIC? [L1] 3. Explain the semi-custom and full-custom styles of VLSI System Design. 4. What are different types of integrated circuits? 5. Explain the gate-array based VLSI system design. 6. Explain the standard cell based VLSI system design.
Remarks, if any

MODULE: 1 Title: **Introduction to VLSI Design** Day 4, Friday, Date: 05.08.16 [2.10pm to 3.00pm]
CONTENTS Programmable Logic Devices. PAL
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To understand the operation of Programmable logic devices. 2. To implement different functions using PAL
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Realize 1 bit full adder circuit using PAL. [L3]
Remarks, if any

MODULE: 1 Title: **Introduction to VLSI Design** Day 5, Tuesday, Date: 09.08.16 [11.40am to 12.30pm]
CONTENTS Programmable Logic Devices. PLA & PROM.
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To understand the operation of Programmable logic Array and PROM. 2. To implement different functions using PLA & PPROM.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Realize 1 bit full adder circuit using PLA & PROM. [L2, L3]
Remarks, if any

MODULE: 1 Title: **Introduction to VLSI Design** Day 6, Wednesday, Date: 10.08.16 [10.00am to 10.50am]

CONTENTS
CPLD, FPGA

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. To understand the Internal Architecture of CPLD & FPGA.
2. To implement different functions using CPLD & FPGA.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):
1. Explain the basic building block of FPGA with diagram [L1]
2. Explain the basic building block of CPLD with diagram [L2]
3. Implementation of a function using CPLD & FPGA. [L2, L3]

Remarks, if any

MODULE: 1
Title: **Introduction to VLSI Design**
Day 7, Thursday, Date: 11.08.16 [2.10pm to 3.00pm]

CONTENTS
Design principles (Digital VLSI –Concept of Regularity, Granularity, modularity, Localityetc)

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. To understand the concept of Regularity, Granularity, modularity, Locality.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):
1. What are regularity, Granularity,modularity and Locality? [L1]
2. What are their significances in modern IC technology? [L2]

Remarks, if any

MODULE: 1
Title: Introduction to signal and systems
Day 8, Friday, Date: 12.08.16 [2.10pm to 3.00pm]

CONTENTS
Different Design Domains (Behavioral, Structural, Physical etc.)

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. To understand the VLSI Design Domains.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Draw the Y-Chart and explain the VLSI design process. [L1]
2. What do you mean by Hierarchical Abstraction?

Remarks, if any

MODULE: 2
Title: **Micro-electronic Processes for VLSI Fabrication**

Day 9, Tuesday, Date: 16.08.16 [11.40am to 12.30pm]
CONTENTS Silicon Semiconductor Technology- AnOverview, Wafer processing, Oxidation, Epitaxial deposition, Ion-implantation & Diffusion.
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To understand the basics of Silicon Semiconductor Technology.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Explain the fabrication of SiO_2 using wet oxidation technique. Explain the relative merits and demerits over the dry one [L2] 2. List the processes for fabrication of VLSI circuits. [L1] 3.Discuss the chemical vapour deposition process for VLSI. [L1] 4. Describe the Si oxidation mechanism. What are the uses of SiO_2in VLSI circuits[L1]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 10, Wednesday, Date: 17.08.16.15 [10.00am to 10.50am]
CONTENTS Cleaning, Etching, Photo-lithography – Positive & Negative photo-resist.
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To understand the basics of Silicon Semiconductor Technology.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What is meant by a clean room class? [L2] 2. Describe briefly how you can achieve the desired clean room condition necessary for IC fabrication. [L2] 3. Compare wet etching and dry etching. [L2] 4. What are different types of lithography process? [L1] 5. Discuss the various steps of wafer preparation. [L1]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 11, Thursday, Date: 18.08.16 [2.10pm to 3.00pm]
CONTENTS Basic CMOS Technology – (Steps in fabricating CMOS)
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the basic steps involved in fabricating CMOS.
Once the student has completed this topic/ chapter he/she will be able to answer following

questions/perform the following activities with Levels of Bloom's Taxonomy):
1. Explain with neat diagram the basic steps involved in fabrication Process flow[L3]
2. Why is metallization needed in the final step of IC fabrication? What materials are suitable for this purpose? [L3]

Remarks, if any

MODULE: 2
Title: **Micro-electronic Processes for VLSI Fabrication**
Day 12, Friday, Date: 19.08.16 [2.10pm to 3.00pm]

CONTENTS
Basic n-well CMOS process

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. Understand the basic steps involved in fabricating NMOS process.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):
1. Describe how anMOS device is fabricated? Use diagram to show the steps. [L2]
2. What are the uses of poly-Si? [L2]
3. How is metallization done in VLSI fabrication? [L2]

Quiz Based on CO1:

i. What is meant by the term VLSI?
A device containing between
(b) 10^3 and 10^5 transistors
(c) 10^7 and 10^9 transistors
10^5 and 10^7 transistors
(d) 10^9 and 10^{11} transistors

ii. Subthreshold operation occurs in
(c) Strong inversion region
(c) Saturation region
(d) Weak inversion region
(d) Cut-off region

Remarks, if any

MODULE: 2
Title: **Micro-electronic Processes for VLSI Fabrication**
Day 13, Tuesday, Date: 23.08.16 [11.40am to 12.30pm]

CONTENTS
Basic n-well CMOS process

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. Understand the basic steps involved in fabricating n-Well CMOS process

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Draw the device structure of CMOS Inverter. [L2] 2. Show the different steps to fabricate a CMOS Inverter [L2]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 14, Wednesday, Date: 24.08.16 [10.00am to 10.50am]
CONTENTS p-well CMOS process
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the basic steps involved in fabricating p-Well CMOS process
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Draw the device structure of CMOS Inverter. [L2] 2. Show the different steps to fabricate a CMOS Inverter [L2]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 15, Friday, Date: 26.08.16 [2.10pm to 3.00pm]
CONTENTS Twin tub Process
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the basic steps involved in fabricating Twin-Tub CMOS process
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Draw the device structure of CMOS Inverter. [L2] 2. Show the different steps to fabricate a CMOS Inverter [L2]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 16, Tuesday, Date: 30.08.16 [11.40am to 12.30pm]
CONTENTS Twin tub Process
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the basic steps involved in fabricating Twin-Tub CMOSprocess.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Draw the device structure of CMOS Inverter. [L2] 2. Show the different steps to fabricate a CMOS Inverter [L2]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 17, Wednesday, Date: 31.08.16 [10am to 10.50am]
CONTENTS Layout Design Rule
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand how to design the layout of a circuit following the design rule.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What is DRC in context of layout design?[L2] 2. Discuss the design rules in details. [L2]
Remarks, if any

MODULE: 2 Title: **Micro-electronic Processes for VLSI Fabrication** Day 18, Thursday, Date: 01.09.16 [2.10pm to 3.00pm]
CONTENTS Stick diagram with examples
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the basic concepts of Stick diagram.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What do you mean by DRC, LVS and extraction? [L2] 2. What is Stick diagram? Draw the stick diagram of CMOS 3-input NAND gate. [L3] 3. Draw the stick diagram of CMOS 2-input XOR gate. [L3]
Remarks, if any

MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 19, Friday, Date: 02.09.16 [2.10pm to 3.00pm]
CONTENTS CMOS inverter characteristics
Topic/Unit/Chapter Objectives:

Broad Objectives of the chapter/topic are:
1. Understand the operation of CMOS Inverter.
2. Understand the Voltage Transfer characteristics of CMOS Inverter.
3. Understand the Layout, power and area requirement

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):
1. Explain the operation of CMOS Inverter circuit [L2]
2. Show the Voltage Transfer Characteristic. [L2]

Quiz Based on CO2:

3. Material used for the fabrication of gate in modern MOSFET is
   (c) Highly pure si (c) Epitaxial Si
   (d) Highly pure SiO_2 (d) Highly doped polysilicon
4. Photo-etching is a process of
   (c) Selective removal of layer (c) Removal of photo-resist
   (d) Diffusion of impurities (d) Making dicing marks

Remarks, if any

MODULE: 3
Title: **CMOS for Digital VLSI Circuits**
Day 20, Tuesday, Date: 06.09.16 [11.40am to 12.30pm]

CONTENTS
CMOS inverter characteristics

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. Understand the calculation of different parameters and design of CMOS inverter.
2. Understand the Noise Immunity and Noise Margin.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):
1. What is noise immunity and noise margin? [L1]
2. How to calculate the different voltages involved to draw the Voltage Transfer Characteristics. [L2]
3. How to design a CMOS Inverter? [L2]
4. Draw the Layout and Stick diagram of CMOS Inverter. [L3]

Remarks, if any

MODULE: 3
Title: **CMOS for Digital VLSI Circuits**
Day 21, Wednesday, Date: 07.09.16 [10am to 10.50am]

CONTENTS
NAND & NOR Gates

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. Understand the design procedure for implementing CMOS NAND and NOR gates.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. How to design CMOS Logic gates? [L2] 2. Draw the Layout and Stick diagram of CMOS NAND and NOR gates.[L3]
Remarks, if any

MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 22, Thursday, Date: 08.09.16 [2.10pm to 3.00pm]
CONTENTS CMOS logic circuits
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the design procedure for implementing CMOS logic circuits.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. How to design any CMOS Logic circuits? [L3] 2. Draw the Layout and Stick diagram of CMOS Logic gates and simple logic circuits. [L3]
Remarks, if any

MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 23, Friday, Date: 09.09.16 [2.10pm to 3.00pm]
CONTENTS Complex logic circuits
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the design procedure for implementing Complex CMOS logic circuits.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Draw the Layout and Stick diagram of CMOS complex logic circuits. [L3]
Remarks, if any

MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 24, Tuesday, Date: 13.09.16 [11.40am to 12.30pm]
CONTENTS Complex logic circuits.
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Knowledge on designing complex logic circuits
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Draw the Layout and Stick diagram of CMOS complex logic circuits. [L3]
Remarks, if any
MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 25, Wednesday, Date: 14.09.16 [10.00pm to 10.50am]
CONTENTS CMOS Full Adder
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the design procedure for implementing CMOS Full Adder Circuit. 2. Simplification of designing by using suitable techniques
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Design a CMOS Half Adder Circuit. [L3] 2. Draw the CMOS full adder circuit and explain its operation. [L3] 3. Draw Stick diagram of CMOS complex logic circuits. [L3]
Remarks, if any
MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 26, Thursday, Date: 15.09.16 [2.10pm to 3.00pm]
CONTENTS CMOS Transmission GATE
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the operation of Transmission GATE 2. Reduction of the complexity using transmission gate technology. 3. Knowledge on designing complex logic circuits using transmission gate
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Realize a 2:1MUX using CMOS Transmission gate. [L5] 2. Design two inputs X-OR gate using CMOS Transmission gate. [L5] 3. Realize a function using CMOS Transmission gate. [L5]
Remarks, if any
MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 27, Friday, Date: 16.09.16 [2.10pm to 3.00pm]
CONTENTS Sequential CMOS logic circuits, SR Latch circuit
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the design procedure for implementing Sequential CMOS logic circuits.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Design a CMOS NAND Based SR Latch Circuit. [L3]
Remarks, if any
MODULE: 3 Title: **CMOS for Digital VLSI Circuits** Day 28, Tuesday, Date: 27.9.16 [11.40am to 12.30pm]

CONTENTS
Sequential CMOS logic circuits, SR Latch circuit

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:
1. Understand the design procedure for implementing Sequential CMOS logic circuits.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Design a CMOS NOR Based SR Latch Circuit. [L3]

Remarks, if any

MODULE: 3
Title: **CMOS for Digital VLSI Circuits**
Day 29, Wednesday, Date: 28.9.16 [10.00pm to 10.50am]

CONTENTS
Clocked JK Latch/ Master-Slave JK

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the design procedure for implementing CMOS Clocked JK Latch/ Master-Slave JKFF Circuit.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Design a CMOS NAND Based Clocked JK Latch/ Master-Slave JK FF Circuit. [L3]

Remarks, if any

MODULE: 3
Title: **CMOS for Digital VLSI Circuits**
Day 30, Thursday, Date: 29.09.16 [2.10pm to 3.00pm]

CONTENTS
CMOS D-latch & Edge triggered flip-flop

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the design procedure for implementing CMOS Clocked JK D FF Circuit.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Realize a D FF using CMOS Transmission gate. [L6]

Remarks, if any

MODULE: 4
Title: **Analog VLSI Circuits**
Day 31, Tuesday, Date: 04.10.16 [11.40am to 12.30pm]

CONTENTS
Analog VLSI design steps, Basic building blocks of Analog VLSI chips

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the design steps involved in designing Analog VLSI processes.
2. Understand the Basic building blocks of Analog VLSI chips.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. What are the different steps involved in designing analog IC? [L1]
2. What are the Basic building blocks of Analog VLSI chips? [L1]

Remarks, if any
MODULE: 4 Title: **Analog VLSI Circuits** Day 32, Wednesday, Date: 05.10.16 [10.00pm to 10.50am]
CONTENTS MOS switch, Active load / resistors; Voltage dividers
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. To gather the Knowledge of using the MOSFET as a switch, resistor. 2. To understand the operation of voltage divider.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. What is a MOS switch? [L2] 2. How is it different from CMOS switch? [L4] 3. Draw the resistance characteristics of the CMOS switch. [L3] 4. What is MOS diode/active resistor? [L1] 5. Draw the small signal equivalent circuit and find the expression for output resistance. [L5] 6. Explain with circuit diagram and necessary expressions how voltage division is achieved using MOS circuits. [L4]
Remarks, if any
MODULE: 4 Title: **Analog VLSI Circuits** Day 33, Tuesday, Date: 18.10.16 [11.40am to 12.30pm]
CONTENTS CMOS Current source & sink
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the Characteristics of CMOS Current source &sink. 2. To apply the technique to increase the output resistance. 3. Understand the operation of cascade current sink.
Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy): 1. Explain how a MOSFET can be used as Current source & sink. [L4] 2. Explain the operation of the MOS current reference circuit with circuit diagram. [L3] 3. How the output resistance of current sink can be increased? [L5] 4. Draw the equivalent circuit of cascade current sink and explain its operation. [L2]
Remarks, if any
MODULE: 4 Title: **Analog VLSI Circuits** Day 34, Wednesday, Date: 19.10.16 [10.00pm to 10.50am]
CONTENTS Current Mirror
Topic/Unit/Chapter Objectives: Broad Objectives of the chapter/topic are: 1. Understand the operation of Current mirror circuit 2. Understand the deviation from ideal situation 3. Realization of cascade current mirror

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. What is the principle of operation of a current mirror? [L2]
2. How the circuit is affected due to deviation from ideal situation. [L5]
3. What is the principle of operation of a cascade current mirror? [L2]

Remarks, if any

MODULE: 4

Title: **Analog VLSI Circuits**

Day 35, Thursday, Date: 20.10.16 [2.10pm to 3.00pm]

CONTENTS

CMOS Differential amplifier

Topic/Unit/Chapter Objectives:

Broad Objectives of the chapter/topic are:

1. Understand the operation of CMOS differential amplifier.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Draw the CMOS differential amplifiercircuit and explain how it works as a differential amplifier? [L2]

Quiz Based on CO3:

iii. AND terms are realized by which connections of NMOS in PDN

(c) Series (c) parallel

(d) Cascade (d) Either Series or Parallel

iv. Which one effect does not cause any deviation of a Current Mirror circuit from the ideal situation?

(c) Channel length modulation (c) imperfect geometrical matching

(d) Threshold offset between the two transistors (d) DIBL effects

Remarks, if any

MODULE: 4

Title: **Analog VLSI Circuits**

Day 36, Friday, Date: 21.10.16 [2.10pm to 3.00pm]

CONTENTS

Output amplifiers

Topic/Unit/Chapter Objectives:

Broad Objectives of the chapter/topic are:

1. Understand the operation of Output amplifier.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. What are purposes of an output amplifier? [l2]
2. What are the implementation schemes? [L4]

Quiz Based on CO4:

i. The full form of VHDL is

(a) Very High Digital Logic (b) Verilog Hardware Description Language

(c) Very High Speed Digital Logic (d) None of these

ii. In VHDL, Sequential statements are defined in the

(a) Architecture (b) Process (c) Package (d) None of these

Remarks, if any

MODULE: 4
Title: **Analog VLSI Circuits**
Day 37, Tuesday, Date: 25.10.16 [11.40am to 12.30pm]

CONTENTS
CMOS OPAMP

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the basic building blocks of CMOS OPAMP.
2. Compensation of CMOS OPAMP and its use.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. What are basic building blocks of CMOS OPAMP? Draw them. [L3]
2. What is compensation of CMOS OPAMP and why is it used?

Remarks, if any

MODULE: 4
Title: **Analog VLSI Circuits**
Day 38, Wednesday, Date: 26.10.16 [10.00pm to 10.50am]

CONTENTS
Resistor Realization using Switched capacitor

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the operation of a switched capacitor.
2. Purpose of using switched capacitor instead of a resistor.
3. Realization of resistor using switched capacitor.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Realize a resistor using switched capacitor. [L5]
2. What are the basic advantages and limitations of a switched capacitor? [L5]
3. Explain the working of a switched capacitor first order LPF with circuit diagram. [L3]

Remarks, if any

MODULE: 4
Title: **Analog VLSI Circuits**
Day 39, Thursday, Date: 27.10.16 [2.10pm to 3.00pm]

CONTENTS
Switched capacitor Filter

Topic/Unit/Chapter Objectives:
Broad Objectives of the chapter/topic are:

1. Understand the design steps involved in designing switched capacitor filter.
2. Understand the operation of switched capacitor filter.

Once the student has completed this topic/ chapter he/she will be able to answer following questions/perform the following activities with Levels of Bloom's Taxonomy):

1. Explain the working of a switched capacitor first order LPF with circuit diagram. [L3]

Quiz Based on CO5:

i. In VHDL, Components must be declared

(e) Within the architecture body

(f) Anywhere in the program

(g) In a separate VHDL file

(h) Within the entity declaration

ii. The if-else statements must be

(e) Within a process block

(f) Within the architecture body

(g) Under the entity declaration

(h) Within a while loop

Remarks, if any

(x) Teaching Strategy/Method

- **Learning by Recapitulating** the previous knowledge and understanding the topic based on memorizing them. If students fail to give any answer of the questions from the previous semesters it is advised to cover the topics from books, internet or any other resources. Sometimes video lecture, NPTEL study materials are very much useful for the students to clear their doubt. So resources are provided them to gather knowledge. Students share their knowledge through verbal discussion or by using social networks keeping in mind that "it is easy to gather knowledge but it is not so easy to assimilate". Sharing of knowledge can increase the level of knowledge.
- **Drawing suitable Analogy**: Wherever necessary analogy helps the students to make them understand in better way.
- **Solving the numerical problems** not only engage the students but also help them to think, understand and write the topic. Doubts are cleared during solving a problem.
- **Simulation** through EDA tools validates the theoretical knowledge. Sometimes the students expect the result of the theoretical part by simulating the circuit or any model. In this way their interest level may be uplifted.
- **Question and Answer sessions** clears the doubts. If the questions are repeatedly asked and the answers are also discussed repeatedly the weak students can remember them very easily. Next time they will be able to answer.

(xa) Strategy to support weak students

- Forming a pair with the bright students
- Reviewing the real problem sympathetically. Motivating them to do the classes regularly and encouraging by floating easy questions in the theory classes.
- Advising them for getting additional help from teachers as well as bright student.
- Providing continuous assistance.
- Additional doubt clearing sessions (Beyond Class hours)

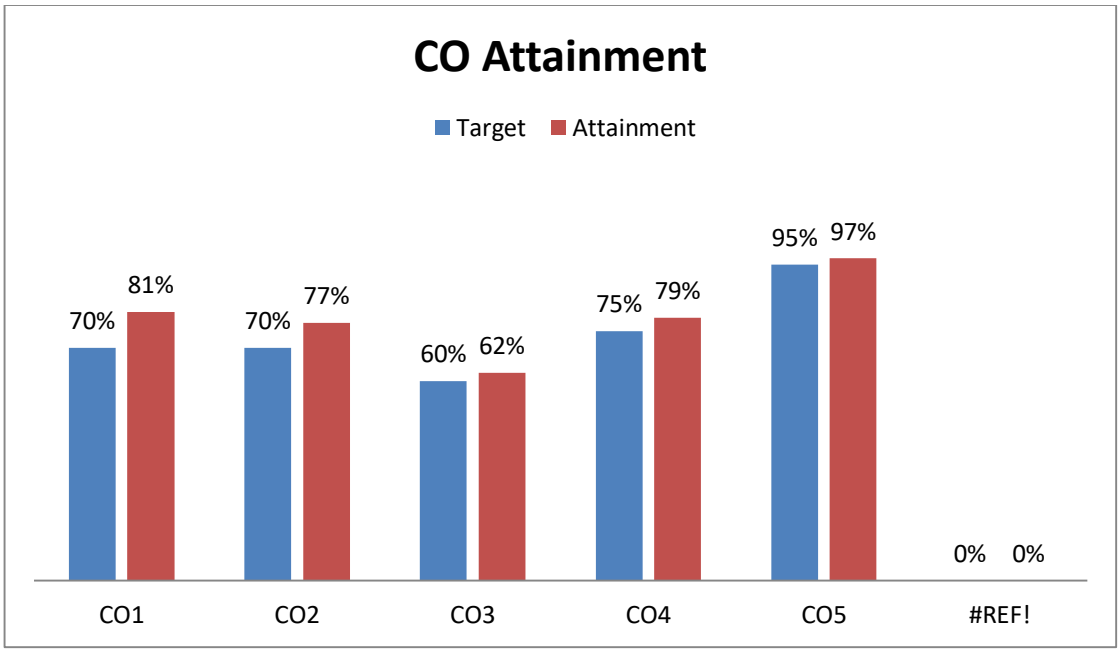
(xb) Strategy to encourage bright students

- Involving them to solve complex numerical problems.
- Motivate them to write paper for publications. Thus they got the knowledge about the topic and know the emerging technologies, find the gap and try to bridge it.
- Giving Board work or power point presentation on a given topic.
- Bright students are involved to boost up the weak students. Sometimes it is the measuring parameter for the bright students that how much extent they can lift the weak students.

(xc) Efforts to keep students engaged

- Giving numerical problem or writing something on a topic and finally the copies are checked by other students arbitrarily chosen. The accepted answer will be finally explained by few of them.
- Providing Questionnaire session. Any student may be asked to answer the question. Other students will be randomly chosen to justify the answers.
- To write the questions they may have and try to find out the solutions after discussion among them.

(xi) Analysis of Students performance in the course (Internal Results)



- 81% students have attained the set target of 70% marks for CO1
- 77% students have attained the set target of 70% marks for CO2
- 62% students have attained the set target of 60% marks for CO3
- 79% students have attained the set target of 75% marks for CO4
- 97% students have attained the set target of 95% marks for CO5

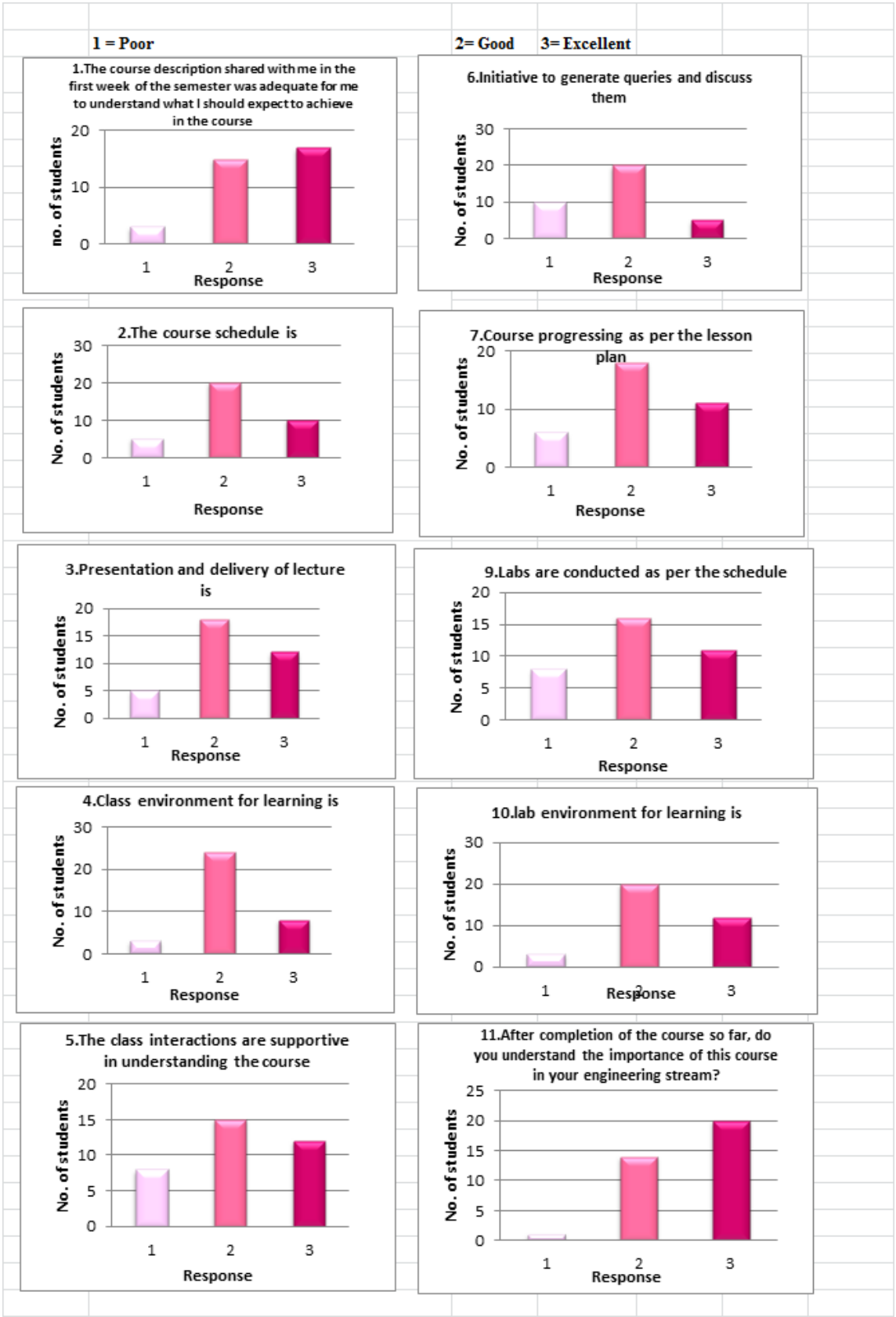
(xii) Analysis of Students performance in the course (University Results)

	Target Course Outcome%	TOTAL STUDENTS	TOTAL STUDENT WHO ATTAINED OUTCOME	% STUDENTS WHO ATTAINED THE OUTCOME
University	70%	**31**	**28**	**90%**

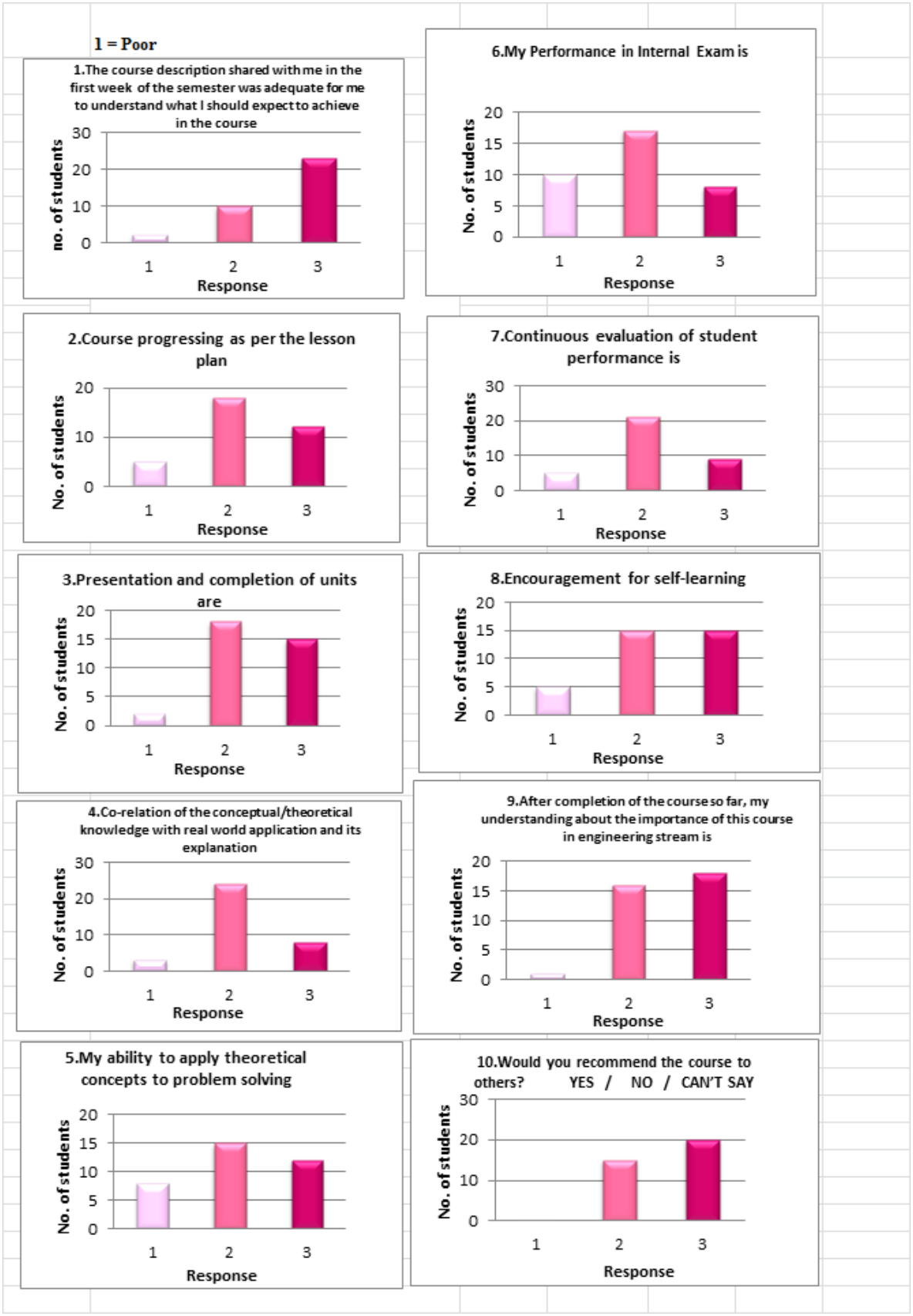
- 90% students have attained the set target of 70% marks for University Exams

(xiii) Analysis of Student Feed Back

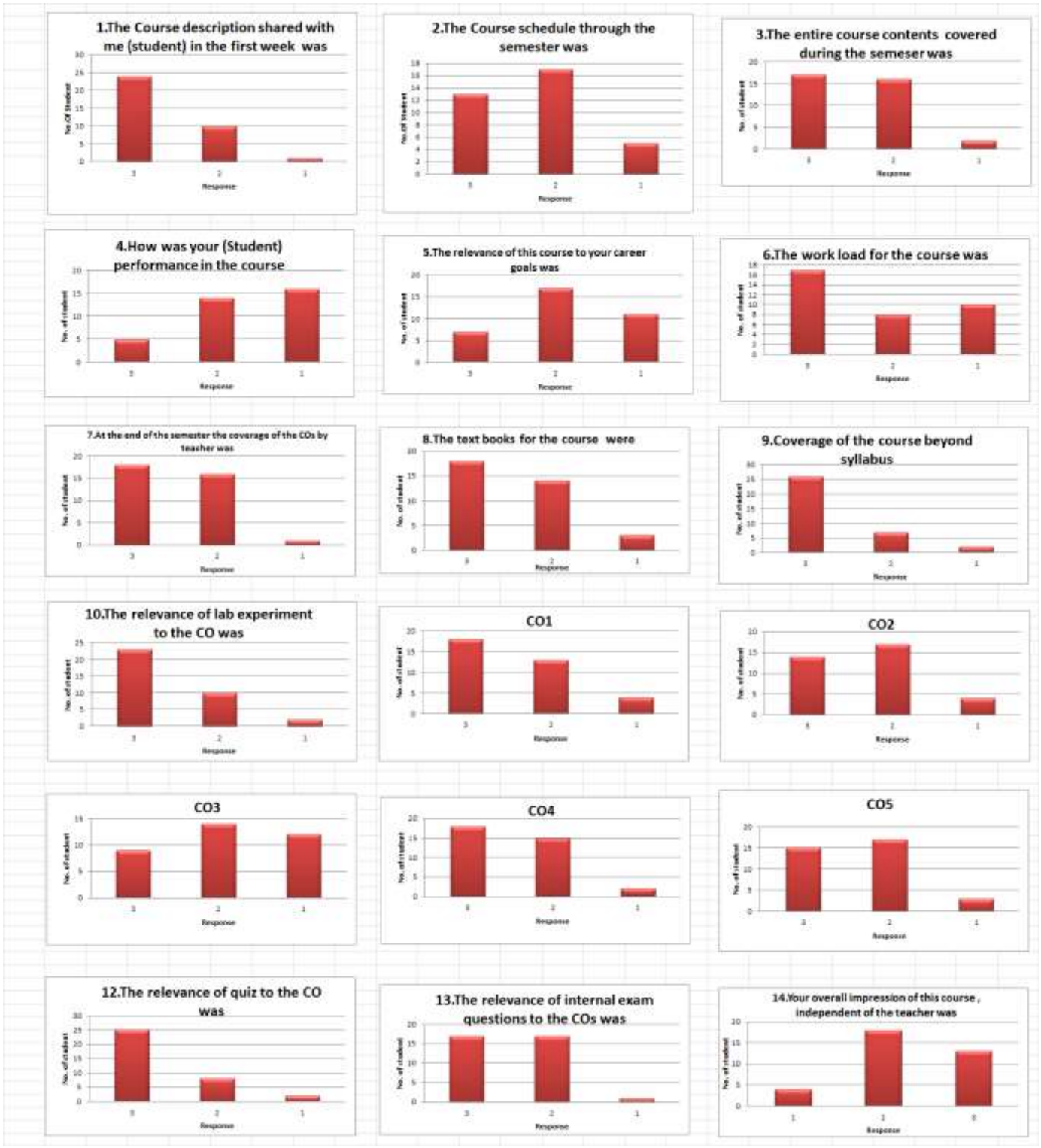
Formative:



Summative:


1 = Poor
1.The course description shared with me in the first week of the semester was adequate for me to understand what I should expect to achieve in the course
no. of students
Response
6.My Performance in Internal Exam is
No. of students
Response
2.Course progressing as per the lesson plan
No. of students
Response
7.Continuous evaluation of student performance is
No. of students
Response
3.Presentation and completion of units are
No. of students
Response
8.Encouragement for self-learning
No. of students
Response
4.Co-relation of the conceptual/theoretical knowledge with real world application and its explanation
No. of students
Response
9.After completion of the course so far, my understanding about the importance of this course in engineering stream is
No. of students
Response
5.My ability to apply theoretical concepts to problem solving
No. of students
Response
10.Would you recommend the course to others? YES / NO / CAN'T SAY
No. of students
Response

CO-Based:


1.The Course description shared with me (student) in the first week was
2.The Course schedule through the semester was
3.The entire course contents covered during the semeser was
4.How was your (Student) performance in the course
5.The relevance of this course to your career goals was
6.The work load for the course was
7.At the end of the semester the coverage of the COs by teacher was
8.The text books for the course were
9.Coverage of the course beyond syllabus
10.The relevance of lab experiment to the CO was
CO1
CO2
CO3
CO4
CO5
12.The relevance of quiz to the CO was
13.The relevance of internal exam questions to the COs was
14.Your overall impression of this course , independent of the teacher was

(xiv)Teacher Self-Assessment (at the completion of course)

From the graphical analysis of the results obtained, it can be seen that most of the course outcome have been achieved successfully by the students but the set target for CO 3 has just touched the attainment level due to difficulty in understanding the analog VLSI circuits to which they are exposed for the first time.

(xv) Recommendations/Suggestions for improvement by faculty

- More emphasis should be given to clear the concepts related to Analog VLSI circuits.

INTERNAL ASSESMENT RECORD

Subject with code: ***Microelectronics and VLSI Designs*** **(EC- 702)**

Semester : 7thSem, 2016 Discipline: ELECTRONICS & COMMUNICATION ENGINEERING

S. No.	Name	Roll No.	Attendance		Marks in Internal Test				Quiz (10)	Total (30)
			Total	**Marks (5)**	I (30)	II (30)	Avg. of 2 tests (30)	**Internal Marks (15)**		
1.	ANKITA SINGH	11900313002	78%	5	16	16	16	8	8	21
2.	APURBA ROY	11900313003	75%	5	24	24	24	12	10	27
3.	ARNAV GHOSH	11900313004	81%	5	24	21	22.5	11.25	8	24.25
4.	ARUNDHUTEE DUTTA	11900313005	80%	5	25	21	23	11.5	10	26.5
5.	AVEEK SAHA	11900313006	90%	5	22	23	22.5	11.25	9	25.25
6.	AVERI RAY	11900313007	82%	5	15	14	14.5	7.25	10	22.25
7.	AYANTIKA DEY	11900313008	75%	5	26	27	26.5	13.25	10	28.25
8.	BIKKY ROKA	11900313009	85%	5	20	18	19	9.5	9	23.5
9.	BIKRAM CHAKRABORTY	11900313010	83%	5	20	19	19.5	9.75	9	23.75
10.	DEBABRATA BANERJEE	11900313011	92%	5	25	22	23.5	11.75	8	24.75
11.	DEBASHISH MUKHERJEE	11900313012	80%	5	23	18	20.5	10.25	8	23.25
12.	DHRITIKANA DAS	11900313014	96%	5	23	20	21.5	10.75	10	25.75
13.	DIBAKAR SAHA	11900313015	75%	5	20	20	20	10	10	25

14.	DIPAYAN BHATTACHARYA	11900313016	79%	5	25	22	23.5	11.75	8	24.75
15.	DISHA MANDAL	11900313017	86%	5	22	26	24	12	10	27
16.	KUNDAN KUMAR CHOURASIA	11900313019	89%	5	27	26	26.5	13.25	10	28.25
17.	MANORANJAN KUMAR	11900313020	75%	5	24	21	22.5	11.25	6	22.25
18.	MAYANK KUMAR	11900313021	76%	5	19	24	21.5	10.75	10	25.75
19.	MD NASIR KHAN	11900313022	81%	5	24	23	23.5	11.75	10	26.75
20.	MONA	11900313023	90%	5	21	20	20.5	10.25	8	23.25
21.	MUNNA PRASAD KOIRI	11900313024	82%	5	22	22	22	11	9	25
22.	NAVIN KUMAR	11900313025	85%	5	21	22	21.5	10.75	9	24.75
23.	NIDHI PRIYA	11900313026	75%	5	20	20	20	10	9	24
24.	PANKAJ GUPTA	11900313028	81%	5	25	16	20.5	10.25	9	24.25
25.	PARTHA SARMA	11900313029	85%	5	20	18	19	9.5	7	21.5
26.	PRADYUT DATTA	11900313030	84%	5	21	18	19.5	9.75	8	22.75
27.	PRAGATI KUMARI	11900313031	85%	5	25	24	24.5	12.25	9	26.25
28.	PRAGYA ROY CHOWDHURY	11900313032	83%	5	22	20	21	10.5	9	24.5
29.	PRANOY	11900313033	96%	5	19	23	21	10.5	9	24.5

	DAS									
30.	PRAVEEN KUMAR OJHA	11900313034	95%	5	23	24	23.5	11.75	7	23.75
31.	SOUVIK BOSE	11900314044	75%	5	22	14	18	9	9	23

RECORDS OF QUIZ

Subject with code: *Microelectronics and VLSI Designs* (EC- 702)

&

VLSI Design Lab(EC792)

Semester : 7thSem, 2016 Discipline: ELECTRONICS & COMMUNICATION ENGINEERING

Sl. No	Name	Roll No.	Quiz1	Quiz2	Quiz3	Quiz4	Quiz5
1.	ANKITA SINGH	11900313002	1	1	2	2	2
2.	APURBA ROY	11900313003	2	2	2	2	2
3.	ARNAV GHOSH	11900313004	2	2	1	1	2
4.	ARUNDHUTEE DUTTA	11900313005	2	2	2	2	2
5.	AVEEK SAHA	11900313006	2	2	1	2	2
6.	AVERI RAY	11900313007	2	2	2	2	2
7.	AYANTIKA DEY	11900313008	2	2	2	2	2
8.	BIKKY ROKA	11900313009	2	2	1	2	2
9.	BIKRAM	11900313010	2	2	1	2	2

	CHAKRABORTY						
10.	DEBABRATA BANERJEE	11900313011	1	2	1	2	2
11.	DEBASHISH MUKHERJEE	11900313012	2	2	1	1	2
12.	DHRITIKANA DAS	11900313014	2	2	2	2	2
13.	DIBAKAR SAHA	11900313015	2	2	2	2	2
14.	DIPAYAN BHATTACHARYA	11900313016	1	1	2	2	2
15.	DISHA MANDAL	11900313017	2	2	2	2	2
16.	KUNDAN KUMAR CHOURASIA	11900313019	2	2	2	2	2
17.	MANORANJAN KUMAR	11900313020	1	1	1	1	2
18.	MAYANK KUMAR	11900313021	2	2	2	2	2
19.	MD NASIR KHAN	11900313022	2	2	2	2	2
20.	MONA	11900313023	1	2	1	2	2
21.	MUNNA PRASAD KOIRI	11900313024	2	1	2	2	2
22.	NAVIN KUMAR	11900313025	2	2	1	2	2
23.	NIDHI PRIYA	11900313026	2	2	1	2	2
24.	PANKAJ GUPTA	11900313028	2	1	2	2	2

25.	PARTHA SARMA	11900313029	1	2	1	2	1
26.	PRADYUT DATTA	11900313030	2	1	1	2	2
27.	PRAGATI KUMARI	11900313031	2	1	2	2	2
28.	PRAGYA ROY CHOWDHURY	11900313032	2	2	1	2	2
29.	PRANOY DAS	11900313033	2	1	2	2	2
30.	PRAVEEN KUMAR OJHA	11900313034	1	1	1	2	2
31.	SOUVIK BOSE	11900314044	2	2	2	1	2

LIST OF PRACTICALS

Subject with code: VLSI Design Lab (EC- 792)

Semester : 7thSem, 2016

Discipline: ELECTRONICS & COMMUNICATION ENGINEERING

Sl.	Details of Experiment(s)	Hours allotted
1	Familiarity with Spice simulation tool& EDA tools	6.
2	Spice Simulation of Inverter , NAND , NOR Gates and different analysis using EDA Tools	6
3	Design of CMOS XOR/XNOR Gates and different analysis using EDA Tools	3
4	Design of CMOS Full adder and different analysis using EDA Tools	3
5	Design of CMOS Flip flops (R-S ,D , J-K)and different analysis using EDA Tools	3
6	Design of 8 bit synchronous Counter and different analysis using EDA Tools	3
7	Design of 8 bit bi-directional register and different analysis using EDA Tools	3
8	Design of a 12 bit CPU with few instructions and implementation and validation on FPGA	3

Sessional/Practical Performance Record

Subject with code: VLSI Design Lab (EC- 792)

Semester : 7thSem, 2016 Group: A

Discipline: ELECTRONICS & COMMUNICATION ENGINEERING

Sl.No.	Name	Roll No.	Marks in experimentation								
			1	2	3	4	5	6	7	8	TOTAL (40)
1.	ANKITA SINGH	11900313002	5	4	5	5	4	3	3	2	32
2.	APURBA ROY	11900313003	4	4	5	5	5	5	5	2	35
3.	ARNAV GHOSH	11900313004	4	5	4	5	4	4	4	2	32
4.	ARUNDHUTEE DUTTA	11900313005	4	5	4	4	3	4	4	2	30
5.	AVEEK SAHA	11900313006	4	5	4	4	5	5	4	2	33
6.	AVERI RAY	11900313007	4	5	4	4	4	4	4	2	31
7.	AYANTIKA DEY	11900313008	3	0	3	2	4	4	5	2	23
8.	BIKKY ROKA	11900313009	4	5	5	4	4	4	3	2	31
9.	BIKRAM CHAKRABORTY	11900313010	4	5	5	5	4	3	3	2	31
10.	DEBABRATA BANERJEE	11900313011	4	5	5	5	5	5	5	2	36
11.	DEBASHISH MUKHERJEE	11900313012	4	5	5	5	5	4	4	2	34
12.	DHRITIKANA DAS	11900313014	4	5	5	5	4	5	4	2	34
13.	DIBAKAR SAHA	11900313015	4	5	4	4	4	3	3	2	29
14.	DIPAYAN BHATTACHARYA	11900313016	4	5	5	4	4	5	4	2	33
15.	DISHA	11900313017	4	5	5	4	4	5	3	2	32

	MANDAL										
16.	KUNDAN KUMAR CHOURASIA	11900313019	4	5	5	4	4	5	4	2	33
17.	MANORANJAN KUMAR	11900313020	4	5	5	4	5	5	5	2	35
18.	MAYANK KUMAR	11900313021	4	5	5	5	5	5	5	2	36
19.	MD NASIR KHAN	11900313022	4	5	5	5	5	4	4	2	34
20.	MONA	11900313023	4	5	5	5	4	4	3	2	32
21.	MUNNA PRASAD KOIRI	11900313024	4	5	5	5	5	4	5	2	35
22.	NAVIN KUMAR	11900313025	4	5	4	4	4	4	3	2	30
23.	NIDHI PRIYA	11900313026	4	5	5	5	5	4	4	2	34
24.	PANKAJ GUPTA	11900313028	4	5	4	4	4	4	3	2	30
25.	PARTHA SARMA	11900313029	4	3	3	2	4	3	3	2	24
26.	PRADYUT DATTA	11900313030	4	5	4	4	4	4	3	2	30
27.	PRAGATI KUMARI	11900313031	4	5	5	5	4	4	3	2	32
28.	PRAGYA ROY CHOWDHURY	11900313032	4	3	4	3	4	4	4	2	28
29.	PRANOY DAS	11900313033	4	5	5	5	5	4	3	2	33
30.	PRAVEEN KUMAR OJHA	11900313034	4	5	5	5	5	5	5	2	36
31.	SOUVIK BOSE	11900314044	4	3	3	4	3	4	3	0	24

NAME WITH ROLL Nos. OF STUDENT WHOSE ACADEMIC PERFORMANCE IS NOT SATISFACTORY			
Sl.	**Name of Student**	**Roll No.**	**Remedial measures taken by teacher**
1	BIKRAM CHAKRABORTY	11900313010	• Additional doubt clearing sessions • Providing extra Viva-Voce to students with poor attendance. • Guiding them through previous question papers • Highlighting important and frequently asked questions
2	ANKITA SINGH	11900313002	
3	PARTHA SARMA	11900313029	

CERTIFICATE

I, the undersigned, have completed the course allotted to me as shown below

Sl. No.	Semester	Subject with Code	Total Modules	Remarks
1.	7th	***Microelectronics and VLSI Designs* (EC- 702) &VLSI Design Lab (EC- 792)**	04	

Date :	**Signature of Faculty**

Submitted to HOD

Certificate by HOD

I, the undersigned, certify that **Prof. Manas kumar Parai & Prof. Saroj Mondal** have completed the course work allotted to them satisfactorily/ not satisfactorily.

Date :	**Signature of HOD**

Submitted to Director

Date :	**Signature of Director**